IN THE CLAIMS:

Claims have been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently amended) A method for making a metallization structure for a semiconductor device, comprising:

forming a substantially planar first dielectric layer on a substrate;

forming at least one metal containing barrier layer over the first dielectric layer;

forming a homogenous ~~single~~ conducting layer directly on the at least one metal containing barrier layer;

forming a second dielectric layer in contact with the ~~single~~ homogenous conducting layer;

removing aligned portions of the second dielectric layer, ~~single~~ homogenous conducting layer, and at least one metal containing barrier layer to form a multilayer structure; and

forming metal containing spacers on sidewalls of the multilayer structure, said metal containing spacers beginning at a lower surface of said at least one metal containing barrier layer and extending substantially to an upper surface of said second dielectric layer.

2. (previously presented) The method of claim 1, wherein said forming the first dielectric layer comprises forming a silicon oxide or BPSG layer.

3. (previously presented) The method of claim 2, wherein said forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer of Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

4. (previously presented) The method of claim 3, further comprising forming a second metal containing barrier layer between a first metal containing barrier layer of said at least one metal containing barrier layer and the substrate, said second metal containing barrier layer comprising TiN, TiW, WN, or TaN.

5. (previously presented) The method of claim 1, wherein said forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer of titanium or titanium nitride.

6. (previously presented) The method of claim 1, wherein the at least one metal containing barrier layer is a single metal containing barrier layer and further comprising forming the single metal containing barrier layer of titanium or titanium nitride.

7. (Currently amended) The method of claim 1, wherein said forming the ~~single~~ homogenous conducting layer comprises forming the ~~single~~ homogenous conducting layer from at least one of aluminum and copper.

8. (Currently amended) The method of claim 7, wherein said forming the ~~single~~ homogenous conducting layer comprises forming the ~~single~~ homogenous conducting layer of an aluminum-copper alloy.

9. (previously presented) The method of claim 1, wherein said forming the metal containing spacers comprises forming at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN.

10. (previously presented) The method of claim 9, wherein said forming the metal containing spacers comprises forming the metal containing spacers of titanium or titanium nitride.

11. (Currently amended) The method of claim 1, wherein said forming a second dielectric layer comprises forming the second dielectric layer on the ~~single~~ homogenous conducting layer to have sidewalls aligned with sidewalls of the ~~single~~ homogenous conducting layer, and forming the metal containing spacers to extend along the sidewalls of the second dielectric layer.

12. (previously presented) The method of claim 11, further comprising forming the second dielectric layer of a low dielectric constant material.

13. (previously presented) The method of claim 12, further comprising forming the second dielectric layer of a fluorine-doped silicon oxide.

14. (previously presented) The method of claim 1, further comprising forming the at least one metal containing barrier layer and the metal containing spacers of a same metal.

15. (previously presented) The method of claim 1, wherein said forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer by vapor deposition.

16. (previously presented) The method of claim 1, wherein said forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer by CVD, PVD or PECVD.

17. (Currently amended) The method of claim 1, wherein said forming the ~~single~~ homogenous conducting layer comprises forming the ~~single~~ homogenous conducting layer by vapor deposition.

18. (Currently amended) The method of claim 17, further comprising forming the ~~single~~ homogenous conducting layer by CVD, PVD or PECVD.

19. (previously presented) The method of claim 1, wherein said forming the metal containing spacers comprises forming the metal containing spacers by vapor deposition and directional etching.

20. (original) The method of claim 19, further comprising effecting the vapor deposition as CVD, PVD or PECVD.

21. (Currently amended) The method of claim 1, wherein removing aligned portions of the second dielectric layer, ~~single~~ homogenous conducting layer, and at least one metal containing barrier layer to form the multilayer structure is effected by patterning and etching the second dielectric layer, the ~~single~~ homogenous conducting layer, and the at least one metal containing barrier layer.

22. (previously presented) The method of claim 1, wherein said forming the metal containing spacers comprises forming a metal containing spacer layer over the multilayer structure and first dielectric layer and removing portions thereof overlying the first and second dielectric layers.

23. (previously presented) The method of claim 22, wherein said forming the metal containing spacers comprises forming the metal containing spacer layer over the multilayer structure and first dielectric layer by a conformal deposition process.

24. (previously presented) The method of claim 23, wherein portions of the metal containing spacer layer over the multilayer structure and first dielectric layer are removed by etching.

25. (Currently amended) The method of claim 1, further comprising removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacers laterally adjacent thereto to expose said ~~single~~ homogenous conducting layer.

26. (previously presented) The method of claim 25, further comprising removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacers by etching.

27-71 (canceled)

72. (Currently amended) A method for constructing a metallization structure for a semiconductor device, comprising:

providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer;

creating a homogenous ~~single~~ conducting layer directly over the at least one metal containing barrier layer, said ~~single~~ homogenous conducting layer comprising at least copper or aluminum and comprising an upper surface, said upper surface of said ~~single~~ homogenous conducting layer out of contact with any metal;

removing aligned portions of the ~~single~~ homogenous conducting layer and at least one metal containing barrier layer to form a multilayer structure; and

flanking at least one surface of the multilayer structure with a metal containing spacer, said metal containing spacer initiating at said at least one metal containing barrier layer and extending to substantially the same height as said ~~single~~ homogenous conducting layer.

73. (Currently amended) The method of claim 72, further comprising forming a second dielectric layer in contact with said ~~single~~ homogenous conducting layer.

74. (previously presented) The method of claim 73, wherein said removing further comprises removing aligned portions of said second dielectric layer to form said multilayered structure.

75. (previously presented) The method of claim 73, wherein said flanking at least one surface of the multilayer structure with a metal containing spacer comprises forming a metal containing spacer layer on said second dielectric layer.

76. (previously presented) The method of claim 75, further comprising removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacer layer laterally adjacent thereto.

77. (previously presented) The method of claim 76, wherein said removing any remaining portion is effected by etching.

78. (previously presented) The method of claim 72, wherein said providing a substrate having a first dielectric layer comprises forming said first dielectric layer of a silicon oxide or BPSG layer.

79. (previously presented) The method of claim 72, wherein said providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer of Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

80. (previously presented) The method of claim 79, wherein said forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer of titanium or titanium nitride.

81. (previously presented) The method of claim 72, further comprising forming a second metal containing barrier layer between a first metal containing barrier layer of the at least one metal containing barrier layer and the substrate, said second metal containing barrier layer comprising TiN, TiW, WN, or TaN.

82. (previously presented) The method of claim 72, wherein the at least one metal containing barrier layer is a single metal containing barrier layer and further comprising forming the single metal containing barrier layer of titanium or titanium nitride.

83. (canceled)

84. (Currently amended) The method of claim 72, wherein said creating a ~~single~~ homogenous conducting layer comprises creating the ~~single~~ homogenous conducting layer of an aluminum-copper alloy.

85. (previously presented) The method of claim 72, wherein said flanking comprises forming the metal containing spacer of at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN.

86. (previously presented) The method of claim 85, wherein said forming the metal containing spacer comprises forming the metal containing spacers of titanium or titanium nitride.

87. (previously presented) The method of claim 72, wherein said flanking at least one surface comprises forming said metal containing spacer on sidewalls of said multilayer structure.

88. (previously presented) The method of claim 72, wherein said flanking at least one surface comprises forming said metal containing spacer on a top surface of said multilayer structure.

89. (Currently amended) The method of claim 72, further comprising forming a second dielectric layer on the ~~single~~ homogenous conducting layer to have sidewalls aligned with the conductive layer sidewalls, and forming the metal containing spacer to extend along the sidewalls of the second dielectric layer.

90. (previously presented) The method of claim 89, wherein said forming the second dielectric layer comprises forming the second dielectric layer of a low dielectric constant material.

91. (previously presented) The method of claim 90, wherein said forming the second dielectric layer comprises forming the second dielectric layer of a fluorine-doped silicon oxide.

92. (previously presented) The method of claim 72, further comprising forming the at least one metal containing barrier layer and the metal containing spacer of a same metal.

93. (previously presented) The method of claim 72, wherein said providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer by vapor deposition.

94. (previously presented) The method of claim 93, wherein said forming the at least one metal containing barrier layer by vapor deposition comprises forming the at least one metal containing barrier layer by CVD, PVD or PECVD.

95. (Currently amended) The method of claim 72, wherein said creating a ~~single~~ homogenous conducting layer comprises forming the homogenous conducting layer by vapor deposition.

96. (Currently amended) The method of claim 95, wherein said forming the ~~single~~ homogenous conducting layer by vapor deposition comprises forming the ~~single~~ homogenous conducting layer by CVD, PVD or PECVD.

97. (previously presented) The method of claim 72, wherein said flanking comprises forming the metal containing spacer by vapor deposition and directional etching.

98. (previously presented) The method of claim 97, further comprising effecting the vapor deposition as CVD, PVD or PECVD.

99. (Currently amended) The method of claim 72, wherein removing aligned portions of the ~~single~~ homogenous conducting layer and at least one metal containing barrier layer to form a multilayer structure is effected by patterning and etching the ~~single~~ homogenous conducting layer and the at least one metal containing barrier layer.

100. (previously presented) The method of claim 72, wherein said flanking comprises forming the metal containing spacer by forming a metal containing spacer layer over the multilayer structure and first dielectric layer and removing portions thereof overlying the first dielectric layer and a top portion of said multilayer structure.

101. (previously presented) The method of claim 100, wherein said forming the metal containing spacer layer over the multilayer structure and first dielectric layer comprises forming the metal containing layer by a conformal deposition process.

102. (previously presented) The method of claim 101, wherein said removing portions of the metal containing spacer layer is effected by etching.

103. (Currently amended) A method for making a metallization structure for a semiconductor device, comprising:

forming a substantially planar first dielectric layer on a substrate;

forming at least one metal containing barrier layer over the first dielectric layer;

forming a ~~single~~ homogenous conducting layer ~~over~~ directly on the at least one metal containing barrier layer;

forming a second dielectric layer in contact with the ~~single~~ homogenous conducting layer;

removing aligned portions of the second dielectric layer, the ~~single~~ homogenous conducting layer, and the at least one metal containing barrier layer to form a multilayer structure;

forming metal containing spacers on sidewalls of the multilayer structure, said metal containing spacers originating at said at least one metal containing barrier layer; and

removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacers laterally adjacent thereto.

104. (previously presented) The method of claim 103, wherein said removing any remaining portion is effected by etching.

105. (Currently amended) A method for constructing a metallization structure for a semiconductor device, comprising:

providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer;

creating a homogenous conducting layer directly on the at least one metal containing barrier layer;

forming a second dielectric layer on said homogenous conducting layer;

removing aligned portions of the second dielectric layer, the homogenous conducting layer and the at least one metal containing barrier layer to form a multilayer structure;

flanking at least one surface of the multilayer structure with a metal containing spacer such that said metal containing spacer originates at said at least one metal containing barrier and is substantially the same height as said second dielectric layer; and

removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacer layer laterally adjacent thereto.

106. (previously presented) The method of claim 105, wherein said removing any remaining portion is effected by etching.